Call for Papers:

IEEE Micro Special Issue: High-Speed Data Center Interconnects

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Submissions due: March 7, 2014 **Publication date:** Sep-Oct 2014

The demands being placed upon datacenter networks continue to expand along a number of dimensions. Today's massive datacenters interconnect tens to hundreds of thousands of machines while attempting to deliver high bisection bandwidths and low latency under practical power and cost constraints. Meeting these challenges is becoming increasingly difficult as the port speed of individual server NICs moves past 10 Gbps. Next-generation Ethernet specifications focus on delivering aggregate bandwidth through multiple parallel channels, and call for link rates of 100 Gbps, 400 Gbps, and beyond. Moreover, disruptive changes at the end host such as disaggregated server designs have the potential to dramatically change traffic demands. Designing cost-effective scalable interconnect technologies at these speeds is an open challenge.

Both academic and industrial researchers are actively exploring new control planes that attempt to harness the incredible capacity of these next-generation network fabrics while still delivering reasonable levels of utilization and performance. These approaches are pushing the boundaries of what is currently understood regarding both traditional and software-defined networking (SDN) technologies, including how to leverage fast programmable TCAMs, optical transport, and even on-board server NIC capacity. Designing practical high-speed interconnects to deliver on the promise of next-generation data centers and cloud-based computing calls for new architectural advances. This IEEE Micro special issue seeks original papers on a range of topics related to such interconnects.

Areas of interest include, but are not limited to:

- Highly scalable data center network designs
- Novel and innovative interconnect architectures
- NIC designs supporting 100 Gbps and beyond
- The applicability of merchant silicon to next-generation network designs
- Reliability and fault tolerance in data center networks
- Hybrid interconnect designs, relying on wireless and/or optical circuit switching
- Control planes based on software designed networking (SDN)
- Processor design implications of high-speed data center interconnect

Submission procedure:

Log onto IEEE CS Manuscript Central (https://mc.manuscriptcentral.com/micro-cs) and submit your manuscript. Please direct questions to the IEEE Micro magazine assistant (micro-ma@computer.org). For the manuscript submission, acceptable file formats include Microsoft Word and PDF. Manuscripts should not exceed 5,000 words including references, with each average-size figure counting as 150 words toward this limit. Please include all figures and tables, as well as a cover page with author contact information (name, postal address, phone, fax, and e-mail address) and a 200-word abstract. Submitted manuscripts must not have been previously published or currently submitted for publication elsewhere, and all manuscripts must be cleared for publication. All previously published papers must have at least 30% new content compared to any conference (or other) publication. Accepted articles will be edited for structure, style, clarity, and readability. For more information, please visit the IEEE Micro Author Center (http://www2.computer.org/portal/web/peerreviewmagazines/acmicro)

Important dates:

Initial submissions due:	*March 7, 2014*	Final version due:	*June 23, 2014*
Author notification:	*April 30, 2014*	Publication timeframe:	*Sept-Oct 2014*

Questions? Contact the guest editors: ieee-micro-dc-editors@sysnet.ucsd.edu